STI structures **65** are formed by the following process steps: etching openings into the substrate **40** from the front side **50**; filling the openings with a dielectric material such as silicon oxide, silicon nitride, silicon oxynitride, a low-k material, or another suitable dielectric material; and thereafter performing a polishing process—for example a chemical mechanical polishing (CMP) process—to planarize the surface of the dielectric material filling the openings. In some embodiments, deep trench isolation (DTI) structures may be formed. The formation processes for the DTI structures may be similar to the STI structures **65**, though the DTI structures are formed to have greater depths than the STI structures **65**. In certain embodiments, doped isolation structures may also be formed. These doped isolation structures may be formed by one or more ion implantation processes. The doped isolation structures may be formed to replace or to supplement the STI or DTI structures.

A plurality of pixels is formed in the substrate **40**. The pixels contain radiation-sensing doped regions **70**. These radiation-sensing doped regions **70** are formed by one or more ion implantation processes or diffusion processes and are doped with a doping polarity opposite from that of the substrate **40** (or the doped region **140**). Thus, in the embodiment illustrated, the pixels contain n-type doped regions. For a BSI image sensor device such as the image sensor device **30**, the pixels are operable to detect radiation, such as an incident light **75**, that is projected toward device substrate **40** from the back side **60**.

In some embodiments, the pixels each include a photodiode. A deep implant region may be formed below each photodiode in some embodiments. In other embodiments, the pixels may include pinned layer photodiodes, photogates, reset transistors, source follower transistors, and transfer transistors. The pixels may also be referred to as radiation-detection devices or light-sensors. The pixels may be varied from one another to have different junction depths, thicknesses, widths, and so forth. In some embodiments, each pair of adjacent or neighboring pixels are separated from each other by a respective one of the isolation structures (e.g., STI structures **65**) discussed above. The isolation structures **65** prevent or reduce cross-talk between the pixels.

The device substrate **40** also has an initial thickness **78**, which is measured from the front side **50** to the back side **60**. In some embodiments, the initial thickness **78** is in a range from about 100 microns (um) to about 3000 um, for example between about 500 um and about 1000 um.

Referring now to FIG. **3**, an interconnect structure **80** is formed over the front side **50** of the device substrate **40**. The interconnect structure **80** includes a plurality of patterned dielectric layers and conductive layers that provide interconnections (e.g., wiring) between the various doped features, circuitry, and input/output of the image sensor device **30**. The interconnect structure **80** includes an interlayer dielectric (ILD) and a multilayer interconnect (MLI) structure. The MLI structure includes contacts, vias and metal lines. For purposes of illustration, a plurality of conductive lines **90** and vias/contacts **95** are shown in FIG. **3**, it being understood that the conductive lines **90** and vias/contacts **95** illustrated are merely examples, and the actual positioning and configuration of the conductive lines **90** and vias/contacts **95** may vary depending on design needs and manufacturing concerns.

The MLI structure may include conductive materials such as aluminum, aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten, polysilicon, metal silicide, or combinations thereof, being referred to as aluminum interconnects. Aluminum interconnects may be formed by a process including physical vapor deposition (PVD) (or sputtering), chemical vapor deposition (CVD), atomic layer deposition (ALD), or combinations thereof. Other manufacturing techniques to form the aluminum interconnect may include photolithography processing and etching to pattern the conductive materials for vertical connection (for example, vias/contacts **95**) and horizontal connection (for example, conductive lines **90**). Alternatively, a copper multilayer interconnect may be used to form the metal patterns. The copper interconnect structure may include copper, copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, polysilicon, metal silicide, or combinations thereof. The copper interconnect structure may be formed by a technique including CVD, sputtering, plating, or other suitable processes.

Still referring to FIG. **3**, a buffer layer **100** is formed on the interconnect structure **80**. In the present embodiment, the buffer layer **100** includes a dielectric material such as silicon oxide. Alternatively, the buffer layer **100** may optionally include silicon nitride. The buffer layer **100** is formed by CVD, PVD, or other suitable techniques. The buffer layer **100** is planarized to form a smooth surface by a CMP process.

Thereafter, a carrier substrate **110** is bonded with the device substrate **40** through the buffer layer **100**, so that processing of the back side **60** of the device substrate **40** can be performed. The carrier substrate **110** in the present embodiment is similar to the substrate **40** and includes a silicon material. Alternatively, the carrier substrate **110** may include a glass substrate or another suitable material. The carrier substrate **110** may be bonded to the device substrate **40** by molecular forces—a technique known as direct bonding or optical fusion bonding—or by other bonding techniques known in the art, such as metal diffusion or anodic bonding.

Referring back to FIG. **3**, the buffer layer **100** provides electrical isolation between the device substrate **40** and the carrier substrate **110**. The carrier substrate **110** provides protection for the various features formed on the front side **50** of the device substrate **40**, such as the pixels formed therein. The carrier substrate **110** also provides mechanical strength and support for processing of the back side **60** of the device substrate **40** as discussed below. After bonding, the device substrate **40** and the carrier substrate **110** may optionally be annealed to enhance bonding strength.

Still referring to FIG. **3**, after the carrier substrate **110** is bonded, a thinning process **120** is then performed to thin the device substrate **40** from the backside **60**. The thinning process **120** may include a mechanical grinding process and a chemical thinning process. A substantial amount of substrate material may be first removed from the device substrate **40** during the mechanical grinding process. Afterwards, the chemical thinning process may apply an etching chemical to the back side **60** of the device substrate **40** to further thin the device substrate **40** to a thickness **130**, which is on the order of a few microns. In some embodiments, the thickness **130** is greater than about 1 um but less than about 3 um. It is also understood that the particular thicknesses disclosed in the present disclosure are mere examples and that other thicknesses may be implemented depending on the type of application and design requirements of the image sensor device **30**.

Referring now to FIG. **4**, an anti-reflective coating (ARC) layer **150** is formed over the device substrate **40** from the back side **60**. The ARC layer **150** may be formed by a suitable deposition process, such as CVD, PVD, ALD, or